CLAIMS

I claim:

1. A method of storing data, the method comprising:

storing a first set of data to a first set of contiguous memory locations of a flash memory;

setting at least a first bit of a pointer at a fixed set of memory locations of the flash memory, the at least first bit indicating an address of the first set of contiguous memory locations of the flash memory;

storing a second set of data to a second set of contiguous memory locations of the flash memory;

setting at least a second bit of the pointer, the at least second bit indicating an address of the second set of contiguous memory locations of the flash memory; and

erasing at least the pointer after a last bit in the pointer has been set.

2. The method of claim 1 wherein setting at least a first bit of a pointer comprises setting a single bit whose position in the pointer indicates an offset to the first set of contiguous memory locations.

3. The method of claim 1 wherein setting at least a first bit of a pointer comprises setting a single bit whose position in the pointer indicates an offset to the first set of contiguous memory locations and wherein setting at least a second bit of the pointer comprises setting a next successive single bit in the pointer whose position in the pointer indicates an offset to the second set of contiguous memory locations.

4. The method of claim 1 wherein setting at least a first bit of a pointer comprises setting a least significant bit of the pointer and wherein setting at least a

second bit of the pointer comprises setting a next successive bit in the pointer with respect to the least significant bit in the pointer.

5. The method of claim 1, further comprising:

storing a number of additional sets of data to respective ones of a number of additional sets of contiguous memory locations of the flash memory; and

setting at least a number of additional bits of the pointer, each of the bits indicating an address of a respective one of the additional sets of contiguous memory locations of the flash memory;

6. The method of claim 5 wherein the pointer is a word and the bits in the pointer are set consecutively from a least significant bit to a most significant bit.

7. The method of claim 1 wherein erasing at least the pointer after a last bit in the pointer has been set comprises erasing a sector of the flash memory, the sector containing the pointer, the first set of contiguous memory locations and the second set of contiguous memory locations.

8. The method of claim 1 further comprising:

determining a most recent one of the sets of data upon a power up event.

9. The method of claim 8 wherein the pointer is a word and determining a most recent one of the sets of data upon a power up event comprises:

bit shifting the pointer in an order from a last bit in the pointer to a first bit in the pointer.

10. The method of claim 1 further comprising:

determining a most recent one of the sets of data upon a power up event, and

retrieving the most recent one of the sets of data upon the power up event.

11. A method of emulating an electrically erasable programmable read only memory using a flash memory, the method comprising:

storing successive sets of data to respective ones of a number of locations of a flash memory;

for each of the sets of data, setting at least one respective bit of a number of bits of a pointer stored in the flash memory before storing a next one of the sets of data, the at least one bit indicative of the location in the flash memory at which the respective set of data is stored; and

after a last bit in the pointer has been set, erasing a sector of the flash memory containing the pointer and the stored sets of data.

12. The method of claim 11 wherein setting at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data comprises setting a single bit whose position in the pointer indicates a defined offset to the location of the respective set of data in the flash memory.

13. The method of claim 11 wherein setting at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data comprises for each of a first one of the sets of data through an n^{th} one of the sets of data, setting a single corresponding bit from a first bit to an n^{th} bit whose position in the pointer indicates a defined offset to the location of the respective set of data in the flash memory.

14. The method of claim 11, further comprising:

storing further successive sets of data to respective ones of the number of locations of the flash memory; and

for each of the further sets of data, setting at least one respective bit of the pointer before storing a next one of the further sets of data, the at least one bit indicative of the location in the flash memory at which the respective further set of data is stored.

15. The method of claim 11 wherein storing successive sets of data to respective ones of a number of locations of a flash memory comprises storing a set of data stored in a random access memory upon each of a number of successive power down events.

16. The method of claim 11, further comprising:

determining a most recent one of the sets of data upon an occurrence of a power up event by bit shifting the pointer in an order from a last bit in the pointer to a first bit in the pointer.

17. An apparatus to emulate an electrically erasable programmable read only memory using a flash memory, the apparatus comprising:

a flash memory;

means for storing successive sets of data to respective ones of a number of locations of contiguous memory of the flash memory;

means for setting at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data, before storing a next one of the sets of data, the at least one bit indicative of the location in the flash memory at which the respective set of data is stored; and

means for erasing a sector of the flash memory containing the pointer and the stored sets of data after a last bit in the pointer has been set.

18. An apparatus to emulate an electrically erasable programmable read only memory using a flash memory, the apparatus comprising:

a flash memory;

a processor configured to store successive sets of data to respective ones of a number of locations of contiguous memory of the flash memory; to set at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data, before storing a next one of the sets of data, the at least one bit indicative of the location in the flash memory at which the respective set of data is stored; and to erase a sector of the flash memory containing the pointer and the stored sets of data after a last bit in the pointer has been set.

19. The apparatus of claim 18 wherein the processor is further configured to determine a most recent one of the sets of data upon an occurrence of a power up event by bit shifting the pointer in an order from a last bit in the pointer to a first bit in the pointer.

20. A processor-readable media storing instructions for causing a processor to store data, by:

storing successive sets of data to respective ones of a number of memory locations of a flash memory, each memory location comprising a number of contiguous words;

for each of the sets of data, setting at least one respective bit of a number of bits of a pointer stored in the flash memory before storing a next one of the sets of data, the at least one bit indicative of the memory location in the flash memory at which the respective set of data is stored; and

after a last bit in the pointer has been set, erasing a sector of the flash memory containing the pointer and the stored sets of data.

21. The processor-readable media of claim 20 wherein the instructions cause the processor to set at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data by setting a single bit whose

position in the pointer indicates a defined offset to the location of the respective set of data in the flash memory.

22. The processor-readable media of claim 20 wherein the instructions cause the processor to set at least one respective bit of a number of bits of a pointer stored in the flash memory for each of the sets of data by for each of a first one of the sets of data through an n^{th} one of the sets of data, setting a single corresponding bit from a first bit to an n^{th} bit whose position in the pointer indicates a defined offset to the location of the respective set of data in the flash memory.

23. The processor-readable media of claim 20 wherein the instructions cause the processor to store data, further by:

storing further successive sets of data to respective ones of the number of locations of the flash memory on each of a number of successive power down events; and

for each of the further sets of data, setting at least one respective bit of the pointer before storing a next one of the further sets of data, the at least one bit indicative of the location in the flash memory at which the respective further set of data is stored.

24. The processor-readable media of claim 20 wherein the instructions cause the processor to store data, further by:

determining a most recent one of the sets of data by bit shifting the pointer in an order from a last bit in the pointer to a first bit in the pointer

25. A flash memory storing a data structure, the data structure comprising:

a plurality of sets of contiguous memory; and

a pointer at a fixed location, the pointer comprising a number of bits, each bit indicative of a defined location of a respective one of the sets of contiguous memory.

26. The flash memory of claim 25 wherein the pointer comprises sixteen bits, each bit identifying an offset to a respective one of the sets of contiguous memory.

27. The flash memory of claim 26 wherein the offset is a multiple of a position of the bit in the pointer and a defined offset value.

28. The flash memory of claim 25 wherein a single sector of the flash memory contains both the plurality of sets of contiguous memory and the pointer.